TID Effect in SOI Technology

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I. ABSTRACT

In this paper, a brief overview of TID effect in SOI technology is presented. The introduction of buried oxide(BOX) adds vulnerability to TID effect in SOI transistors because of its large thickness. Also the BOX introduces special charge traps, the delocalized spin centers, which in most cases are positive. The charge buildup in BOX could increase the leakage current in front gate transistor in partially depleted devices and result in the threshold voltage shift and leakage current increase in fully depleted front gate transistor in planar SOI transistors. While in non-planar transistors, the better gate control over the channel introduces higher TID tolerance, especially the Ω shaped gate SOI transistor. Complicated physical mechanisms, band to band tunneling and impact ionization, that are responsible for the front gate leakage current increase even in negative gate bias in FD devices are examined. Also the TID effect shows bias dependence in SOI transistor. This dependence is reduced with increasing gate length. Several hardening techniques of BOX are presented, such as the process techniques and the device design, BUSFET as an example, showing enhancement in TID tolerance.

Index Terms--- Total ionizing dose, silicon on insulator.

II. INTRODUCTION

SOI technology is receiving more and more attention because of its advantage over the conventional bulk CMOS technology, such as the high speed, high density, and low power. Three reasons for developing SOI technology are given in historical [1]. They are radiation

hardness required by the military and space application, performance enhancement for commercial application, and tolerance to short channel effect(SCE) to extend the life of silicon technology.

It has been shown that the TID effect (the threshold voltage shift) is proportional to the square of the gate oxide thickness. With the scaling of silicon technology, the front gate oxide thickness is so thin that TID effect in the front gate transistor is negligible. But the unique Buried Oxide(BOX) in SOI transistors make them different from their bulk correspondence. Because the BOX thickness is usually large, so its effect on the whole transistor is significant.

Recently, three-dimensional devices are getting more and more attention, where multi-gate FinFETs have been introduced. Because multi-gate devices provide better gate control over the channel, the electrical properties of the devices outweigh their corresponding bulk devices. So their TID response is significantly improved[2-3]. Especially the Ω shaped gate FET shows high tolerance to the TID[4].

In this paper, the brief overview of TID effects in SOI technology is presented, including the partially depleted(PD) and fully depleted(FD) planar transistors and double gate(DG) and triple gate(TG) FinFETs. The following parts are organized as follows. The first part introduces the basics about SOI technology, mainly different transistor structures. The second part presents the TID response of SOI transistors. And the next part is the hardening techniques for SOI transistors.

III. SOI TRANSISOR STRUCTURES

A. Planar SOI Transistor Structure

There are two types of planar SOI transistors: the fully depleted and partially depleted transistor [5]as shown in Fig. 1. For a SOI transistor, except for the front gate transistor, there is also a parasitic transistor, the back gate transistor where the wafer contact is its gate, and the buried oxide is the gate oxide. If the body is thin enough that it is fully depleted by the front gate

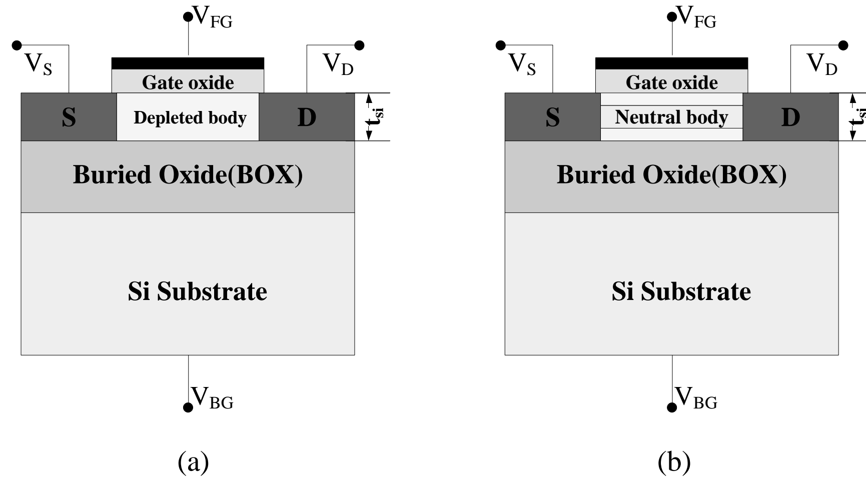


Fig 1. (a) fully depleted SOI transistor; (b) partially depleted SOI transistor[19]

and back gate, so that $t_d(FG) + t_d(BG) \geq t_{Si}$, then it is a fully depleted transistor. Otherwise, as is shown in Fig. 1(b), it is a partially depleted transistor. Because of their different structure, they show different electrical behavior, especially the electrical coupling between front gate and back gate transistor in fully depleted devices.

B. Parasitic Structure model

As is mentioned in part A, the back gate parasitic transistor exists in both kinds of SOI transistors, but they have different behaviors. Except for the parasitic back gate transistor, there is also a parasitic bipolar transistor in partially depleted devices[5]. The floating body acts as the base while the source and drain act as the emitter or collector. This parasitic component could be triggered by proper bias or radiation. Fig. 2 shows the equivalent electrical structure of a SOI transistor.

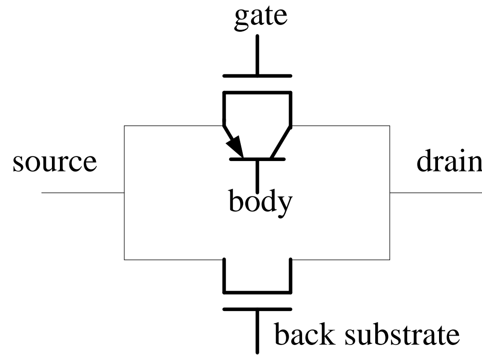
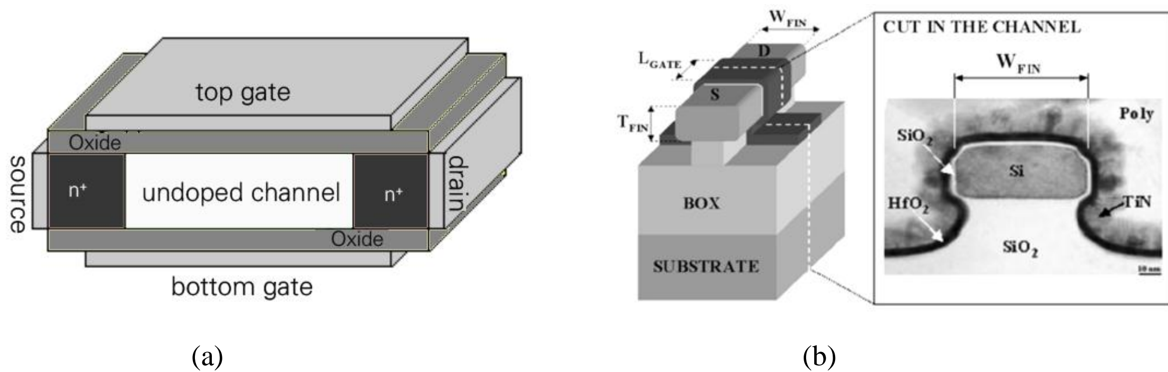


Figure 2 equivalent electrical structure of a SOI transistor[5]

These parasitic components if being triggered, will introduce some degradation to the device characteristics.

C. Non-planar SOI transistor

There are double gate, triple gate or even four gate SOI FinFETs just based on the number of gates. As shown in Fig. 3, the double gate[6] and Ω shaped gate transistor[3] give the



(a) (b)

Figure 3 (a) Double gate FinFET[6]; (b) Ω shaped gate FinFET[3]

example of the multi-gate transistors. For the double gate FinFET, the active silicon area is the fin, and the top and the bottom gate act as the two gate control over the fin. For the Ω shaped gate FinFET, it has three gate control over the thin fin, the top one and the two side ones. In part IV, their structure and their TID response will be analyzed in detail.

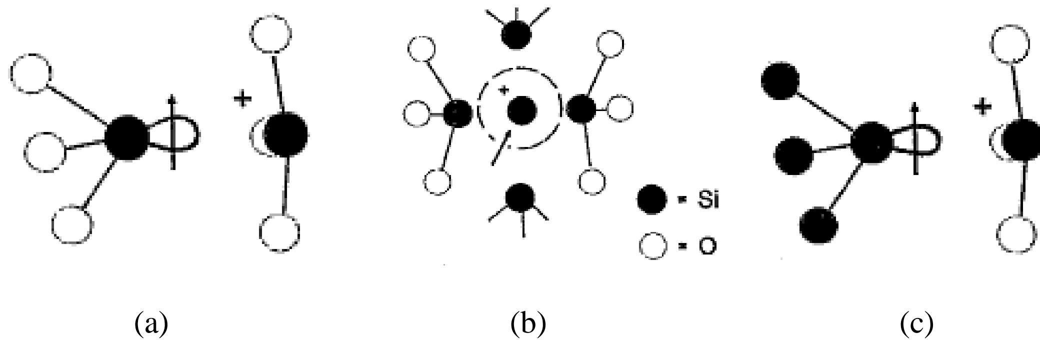
IV. TID RESPONSE OF SOI TECHNOLOGIES

A. Charge Traps

Before showing the specific TID response of different types of SOI transistors, it is necessary to examine the charge traps in the oxide body and the oxide silicon interface. Different charge traps will determine the different TID response. For the bulk transistor, the charge traps have been identified as E' center in the oxide and P_b center in the silicon oxide-silicon interface[7-8]. In SOI transistors, these defects also exist, but there are also unique oxide traps for SOI transistors in the BOX.

Because the E' center and P_b center have been studied in bulk transistors in detail, here only the BOX related charge traps will be examined. The defects that are unique in SOI transistors are delocalized spin centers, where the unpaired electron does not belong to any particular atom. But they are highly fabrication process dependent. There are several leading techniques for SOI wafer fabrication[1]. They are Separation by Implantation of Oxygen (SIMOX) in which the oxide layer is implanted beneath the surface of a Si substrate and Bonded and Etchback SOI(BESOI), where two oxidized wafers are bonded together followed by an etchback of one of the Si substrates to the desired thickness. But nowadays, the BESOI is replaced by Smart Cut technology[20] due to better uniformity it could achieve. However, due to limited specific research on Smart Cut technique, much effort of this paper will be placed on the BESOI which has been characterized for TID effect in detail. It is shown in[9] that the delocalized spin center in SIMOX is E'_δ center, which is characterized as a cluster of 5 Si atoms, as shown in Fig. 4(b), and EH center in BESOI which is characterized as hydrogen related. Also due to different fabrication process, the EH center is likely to be near the bonding interface while the E'_δ center distributes throughout the oxide. It is shown that E'_γ center, D center and the

delocalized spin center are likely to be positive when charges are trapped. But the delocalized spin center is less stable compared with the E'_{γ} center, D center.



(a) (b) (c)

Figure 4 charge traps (a) E'_{γ} center; (b) E'_{δ} center; (c) D center[9]

Besides the former three types of defect centers, the forth kind is oxygen related donor defect in Si substrate[10]. It is suggested that this type of defect may originate from the nonoxidizing or postoxidation anneal during the bonding process.

It is known that the charge buildup in oxide will cause the transistor threshold voltage shift and increase the leakage current in bulk devices, and it is also true for the BOX charge buildup. Next the TID response is shown.

B. Planar SOI Transistor TID Response

The TID response induced by the charge buildup in BOX of partially depleted devices is mainly the increase of leakage current in front gate transistor[5]. Fig. 5 shows the $I-V$ curves of

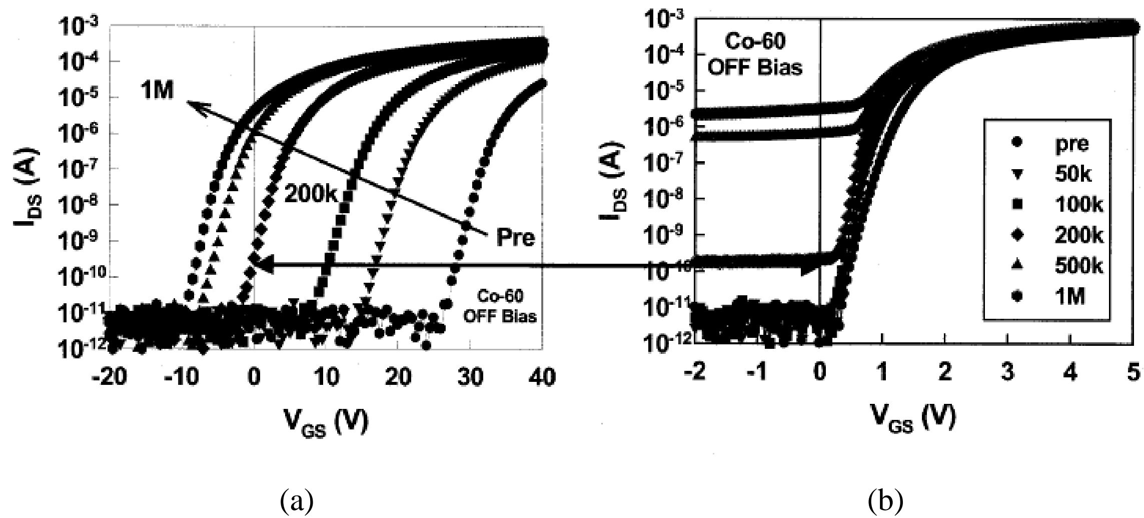


Figure 5 (a) a back gate transistor irradiated up to 1Mrad I-V curve; (b) the top gate transistor leakage current[5]

the back gate transistor and top gate correspondingly. It is biased in the OFF state($V_{DS} = 5V$; other terminals are grounded) when irradiated. Because of the charge buildup in the BOX, the back gate threshold voltage shifts significantly as shown in Fig. 5(a), while the threshold voltage of the top gate negligibly shifts in Fig. 5(b) due to the thin top gate oxide thickness and the lack of electrical coupling between the back gate and top gate transistor.

The existence of electrical coupling between back gate and the top gate transistors makes the fully depleted devices complicated in TID response. Basically, the charge buildup in BOX will cause the increase of leakage current as well as the threshold voltage shift[5][11] in top gate transistor, which is much different from its partially depleted device correspondence. Fig. 6 shows the comparison between fully and partially depleted devices in terms of the threshold voltage shift under irradiation [5]. It's shown that the partially depleted device shows negligible front gate threshold voltage shift while the fully depleted device shows nearly linear coupling between the front gate and back gate.

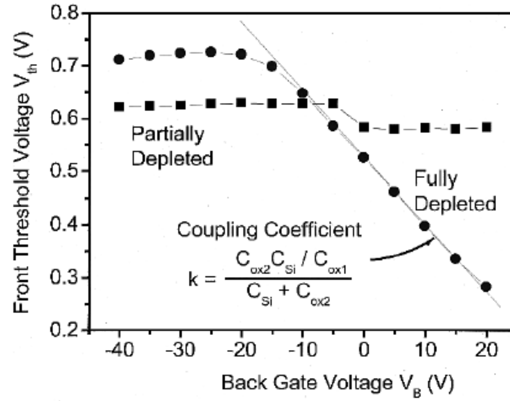


Figure 6 front gate transistor threshold voltage shift versus back gate bias for floating body fully and partially depleted $0.25\mu m$ NMOS transistors[5].

There are some other physical phenomena hide behind that makes the fully depleted device complicated[11]. As shown in Fig. 7, the $I-V$ curve supports three different physical

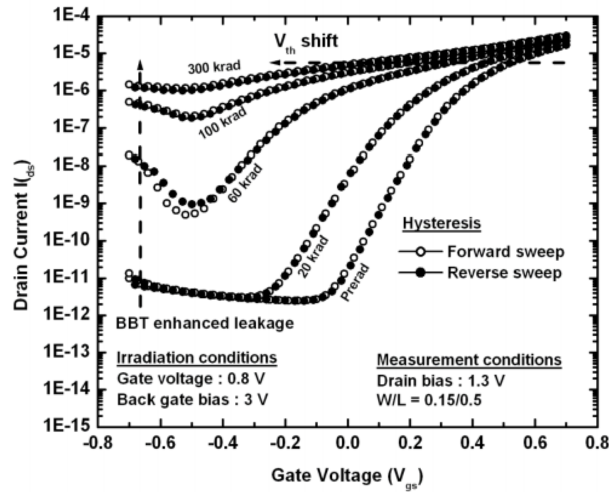
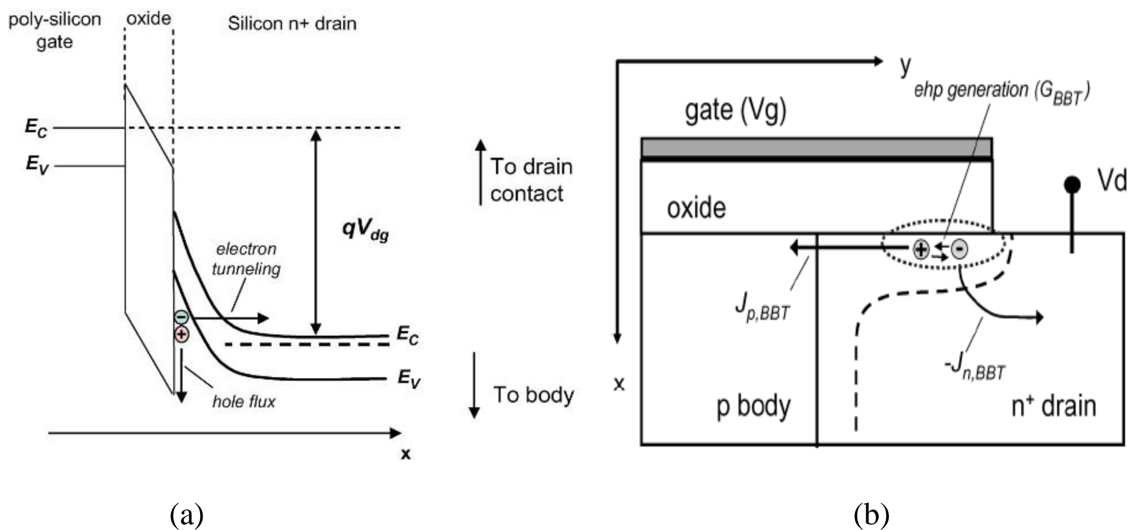


Figure 7 $I-V$ curve under different doses. The device is irradiated under 10kev X-ray at 31.5krad(SiO_2)/min.[11]

phenomena. The first one is the trapped positive charge in NMOS devices, which results in the threshold voltage shift and increase of leakage current in high dose levels. The second one is the impact ionization under moderate irradiation and high drain bias, which causes the increase of leakage current even under negative gate bias. The last one is the band to band tunneling(BBT) under low dose level and moderate drain bias.

At modest dose level and high drain voltage, there is a large electric field existed under the gate drain overlapped region. Electrons in this region will be accelerated by this high field, and in turn, create more electron hole pairs by the avalanche mechanism. The created holes will be swept to the body region, while the electrons to the drain. The body-source junction will be forward biased by these holes possibly which aids the injection of electrons from the source to the body, thus enhancing the parasitic conduction.

Another mechanism (BBT) could be explained in Fig.8[12]. Under low dose level and



(a) (b)

Figure 8 (a) energy band diagram for BBT process; (b)device cross section view of BBT induced current[12]

high drain voltage, the electric field in the drain depletion region is so high that the band bending is large enough that valance band electrons could tunnel into the conduction band. So the leakage current induced by the drain bias is largely increased by this process.

Next the whole picture of current is examined in Fig. 9[12] which contains the physical mechanisms above. Arrow 1 shows the generated holes sweep into the source and body region.

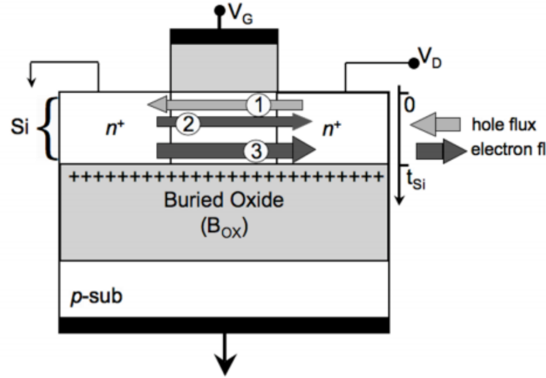


Figure 9 three current process related to the drain degradation[12]

Arrow 2 is the electron injection from the source into the body acting like parasitic bipolar, and the electron sweep by the high electric field in drain depletion region. Arrow 3 represents the charge buildup near the interface of Si and BOX induced leakage current.

C. Non-planar SOI Transistor TID Response

First consider the double gate FinFET[13] TID response. It can be expected to be better than the single gate. For devices in[13], when irradiated under 10keV X-ray source at a dose rate of 31krad(SiO_2)/min, the TID response is shown in Fig. 10. It presents that the double gate device shows less threshold voltage shift than the single gate device which is because of the better gate control over the channel in double gate device.

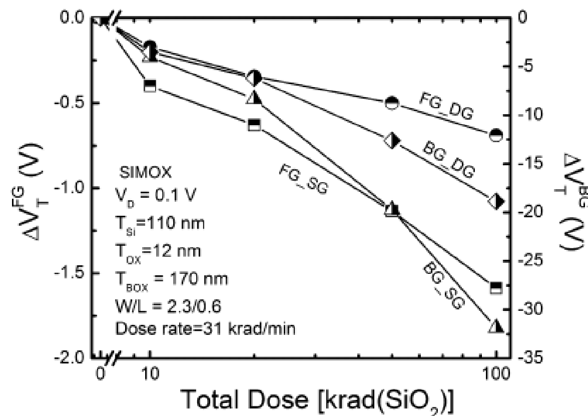
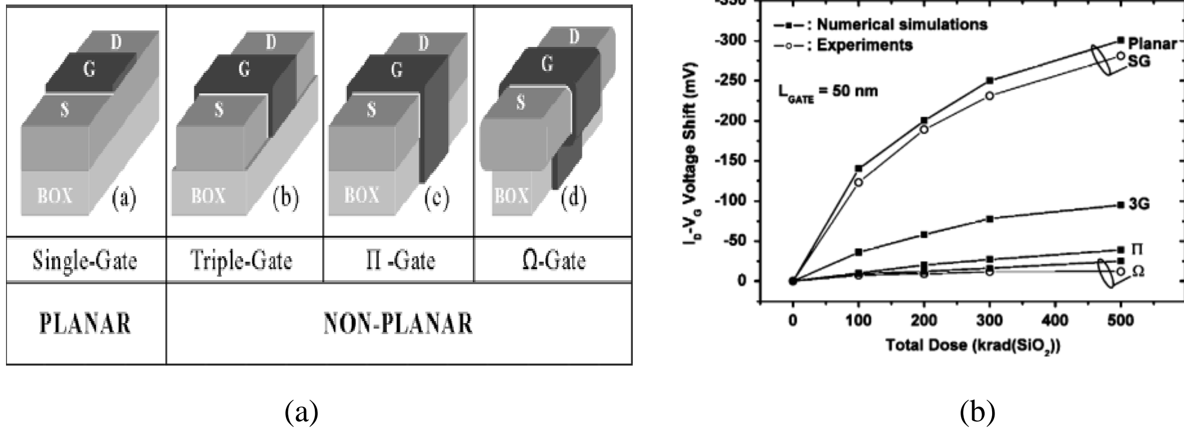


Figure 10 threshold voltage shifts with increasing total dose for a device operating in single and double gate modes[13]

Next the triple gates, especially the Ω gate FinFET shown in Fig. 3(b) are analyzed[3-4]. For the triple gate transistor, its gate control over channel is greatly influenced by the transistor geometry, especially the aspect ratio T_{FIN} / W_{FIN} shown in Fig. 3(b). When the ratio is very small, the two lateral gates are widely apart, thus giving little control over the channel. So, in this condition, the transistor behaves like the single top gate FD transistor. While in the other way, when the ratio is large enough, the two lateral gates are close enough that they show better control over the channel and the electric field could not reach the Si fin/BOX interface, reducing the oxide traps and interface traps. So the TID effect could be expected to be largely improved. Here in Fig. 11(a) shows the schematic configuration of device structures and in Fig. 11(b) shows the simulated results and experimental results.



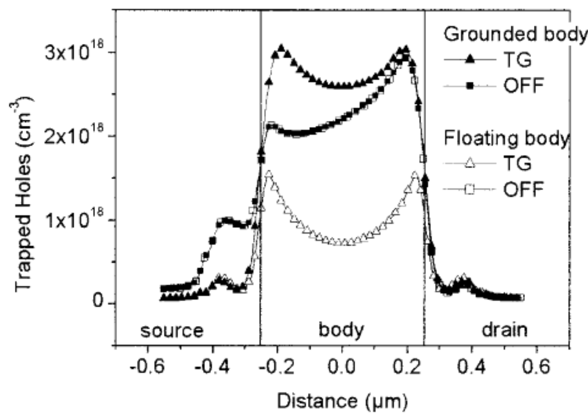
(a) (b)

Figure 11 (a)schematic configuration of device structures (b)simulated voltage shift on the planar single gate(SG), the triple, the Π- and the Ω gate FETs. Also the experimental data are added.[3]

In the Fig. 11(b), up to 500krad(SiO_2), Ω gate FinFET shows negligible threshold voltage shift, while the single gate transistor shows significant threshold voltage shift. This is consistent with the analysis above.

D. Bias Dependence

After the analysis of TID response of different types of SOI transistors, it is interesting to have some understanding of the bias condition[5, 14-15] . Usually the worst case bias is more concerned. The definition of worst case is the bias that could induce the largest threshold voltage shift. And this bias is dependent on the transistor geometry, such as the gate length and the buried oxide thickness. Besides that, the existence of body contact also has very large effect. Because of its simplicity compared with FD devices, PD devices receive exhaustive research[14].



(a)

	S	D	G	B	SUB
ON	0V	0V	V_{DD}	0V	0V
OFF	0V	V_{DD}	0V	0V	0V
TG	V_{DD}	V_{DD}	0V	0V	0V

(b)

Figure 12 (a)trapped holes profile in NMOS with grounded or floating body under different bias conditions; (b)different bias definition[14]

Fig. 12 shows the trapped holes profile in NMOS SOI devices under the TG and OFF state bias. It shows that under OFF state, the body contact has negligible effects on the hole trapping, while it is not the case for TG gate which shows nearly 3 times enhancement with body contact over the device without body contact. A general conclusion about the worst case bias in PD devices is that the largest back gate transistor threshold voltage shift occurs under TG bias with body contact, and under OFF bias with floating body.

The gate length dependence of PD devices with body contact is also included in Fig. 13[14]. The larger the gate length, the smaller the dependence is on the bias condition. Because

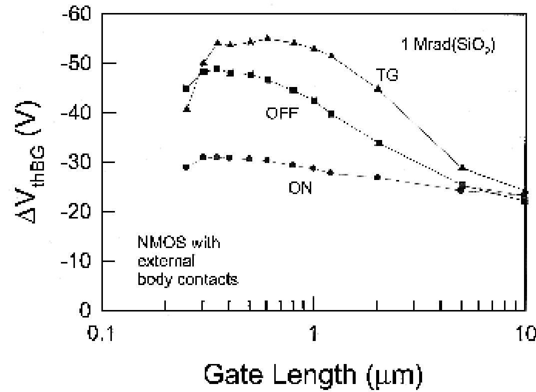


Figure 13 back gate transistor threshold voltage shift versus gate length for a NMOS SOI transistor[14]

for long gate, the bias condition only affects the local areas around the source and drain area, having little effect on the central area under the gate as shown in Fig. 14. The effect of bias

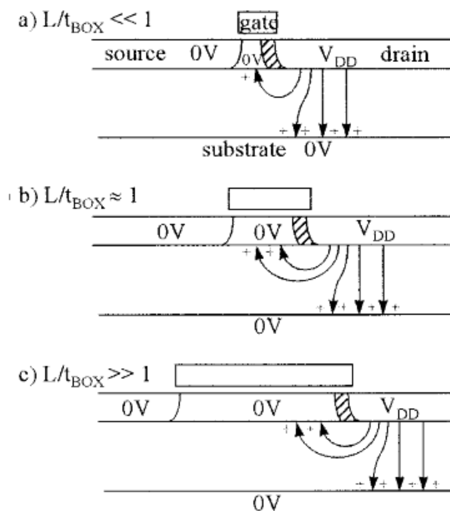


Figure 14 the schematic representation of field lines and hole traps under different L/t_{BOX} ratios for NMOS SOI transistor biased under OFF state[14]

decreases with increasing L/t_{BOX}ratio.

The bias dependence of FD devices is more complicated because of the physical mechanism discussed in part IV and the electrical coupling effect. And it is not well defined. [15]gives a detailed research into this area which this paper will not delve into.

V. TID HARDENING OF SOI TECHNOLOGIES

For the front gate SOI transistor, with the scaling of Si technology, the oxide thickness is continuously shrinking, which provides the best solution to TID effect. However, for the SOI transistor, the introduction of BOX poses another challenge adding the device possible vulnerability to TID effect because of its large thickness. So, the BOX is the part that needs most hardening in SOI transistors.

A. TID Hardening Through Fabrication Process

One Process technique[5, 16] that could be used to harden the SOI transistor is implanting acceptor-like dopants into the BOX, such as silicon, aluminum, or arsenic etc, to create electron traps in the BOX to compensate the hole traps. The generated electrons induced by the irradiation will be captured instead of escaping away from the oxide in the conventional way. So, in this way the SOI transistor is hardened.

For SIMOX fabrication techniques, the hardening of BOX could also be realized by multiple oxygen implantation[5, 17]. This method helps reducing the interface traps and oxide traps. Besides that, the supplemental oxygen implantation[5,18]is also effective in hardening the devices. Because in SIMOX, the defects are usually shallow electron traps, deep hole traps and silicon clusters. After the initial abundant oxygen implantation and high temperature annealing, the additional lower oxygen implantation density and following lower temperature annealing reduce the electron and hole traps and silicon clusters.

B. TID Hardening Through Device Design

Besides the fabrication process techniques, the SOI transistors could also be hardened by careful design of the structure. One example is the body under source field effect transistor(BUSFET)[5], as shown in Fig. 15. The source only extends partially into the silicon

body, so when the charge buildup in the oxide inverts the back channel interface, there is still no conducting path between the source and drain. So, little increase of leakage current will be in the

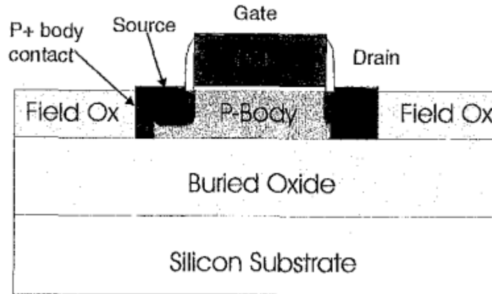


Figure 15 cross section of a BUSFET transistor illustrating a shallow source[5]

front gate transistor. Fig. 16 gives the experimental data that illustrating this point. It shows that

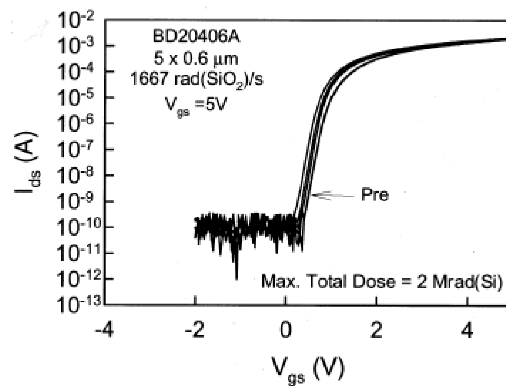


Figure 16 front gate transistor $I - V$ curve after irradiation up to 2Mrad(Si) with Co-60 gamma rays

up to 2Mrad(Si), there is little increase in the leakage current in the front gate transistor. So the BUSFET is quite hard to TID.

VI. CONCLUSION

In this paper, the whole picture of TID effect in SOI transistor is given. First the brief introduction to SOI transistor is given, from the view of geometrical structure and from the view of electrical coupling. Namely the planar SOI transistor and non-planar(FinFET) are introduced.

Next the TID response of SOI transistor is given. The charge traps that are unique for SOI transistor is the delocalized spin center in BOX(E'_{δ} center and EH center). Including the conventional E'_{γ} center, D center, and oxygen related donor center, there are totally four kinds of charge traps in SOI transistor. And the TID effect in planar PD devices is mainly the increase of leakage current in front gate transistor and the threshold voltage shift in the back gate transistor. While for the FD devices, it also includes the threshold voltage shift in the front gate transistor. Because they could provide better gate control over the channel, non-planar FinFETs could have better TID performance than the planar transistors

The electrical coupling and latch effect, the complicated physical mechanisms, in FD devices add more complexity in analyzing the radiation effects. The BBT and impact ionization are responsible for the leakage current increase in low and moderate dose levels and high drain voltage. And the bias dependence of SOI transistor is analyzed. PD devices are easily understood by analyzing the electric field distribution under different bias conditions. This bias dependence decreases with increasing gate length.

Finally the related hardening techniques are presented from the process view to the device design. The hardening techniques could have significant enhancement, just like the BUSFET example.

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