Quartus ii 的使用

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Quartus ii 简介

Quartus II 是<u>Altera公司</u>的综合性PLD/FPGA开发软件,支持原理图、VHDL、 VerilogHDL以及AHDL(Altera Hardware 支持Description Language)等多种设 计输入形式,内嵌自有的综合器以及<u>仿真器</u>,可以完成从设计输入到硬件配 置的完整PLD设计流程。



实验一 QuartusII使用基础

实验目的: 练习逻辑设计原理图输入、编译、选片、设定管脚、编辑仿真文件、功能仿真和时序仿真。

实验内容:

1. 设计、仿真 and3、or3、dff的时序特性。

2. 设计138译码器, 仿真其时序特性。器件选择MAX7128SLC84-7, 指定管脚 按照从小到大的顺序排列。



实验一 QuartusII使用基础

以设计、仿真and3的时序特性为例

步骤:

- 1、新建工程
- 2、原理图输入及编译
- 3、分配管脚
- 4、时序仿真与功能仿真





1、新建一个 project





4



2、设置project放置的位置及其名称,随后按Next继续

What is the working directory for this pro	iject?			
C:\Users\Dongwei\Desktop\PLD\test	1			
What is the name of this project?				
test1				
What is the name of the top-level design entity name in the design file.	n entity for this project?	This name is case s	ensitive and must ex	actly match the
test1				
Use Existing Project Settings	1			





3、添加文件到工程(project)中,在不需要添加的情况下,按Next继续

ne rian	e:					 Add
File	ıame	Туре	Lib	Design entr.	HDL version	Add All
						Remove
						Properties
						Up
						Down
Specify	the path nan	nes of any non-	default libra	ries.	User Libraries	
poony					User Libraries	





4、选择本工程所需要用到的器件MAX7128SLC84-7

			Show in 'Availab	ole device' list-		
Eamily: MAX7000	s		Package:	Any	•	
Devices All			- Pin count	Any	-	
1						
Target device			Speed grade:	Any	-	
C Auto device selected by the Fitter			Show advar	Show advanced devices		
C Specific device selected in 'Available devices' list				omnatible onlu		
zailable devices:						
Vamo	Corou	Maara				
PM7064STC100-7	5.0V	64			^	
PM7064STC100-10	5.0V	64				
7M7064STI44-7	5.0V	64				
PM. 964STI100-7	5.0V	64				
PM712SLC84-6	5.0V	128				
PM7128SLC84-7	5.0V	128				
PM71285LL84-10	5.00	128				
	5.UV	128				
PM71285LL84-15	5.UV	128				
PM71285LU84-15 PM71285LI84-10		128				
PM71285L084-15 PM71285L184-10 PM71285QC100-6	5.UV 5.0V	100				
PM71285LC84-15 PM71285LI84-10 PM71285QC100-6 PM71285QC100-7 PM71285QC100-10	5.0V 5.0V	128				
PM71285L284-15 PM71285L184-10 PM71285QC100-6 PM71285QC100-7 PM71285QC100-10 PM71285QC100-15	5.0V 5.0V 5.0V	128 128 128				
PM71285LL84-15 PM71285L184-10 PM71285QC100-6 PM71285QC100-7 PM71285QC100-10 PM71285QC100-15	5.0V 5.0V 5.0V 5.0V	128 128 128			v	
PM71285LL84-15 PM7128SQC100-6 PM7128SQC100-6 PM7128SQC100-7 PM7128SQC100-10 PM7128SQC100-15 Companion device	5.0V 5.0V 5.0V 5.0V	128 128 128			Ŷ	
PM71285L84-10 PM71285QC100-6 PM71285QC100-7 PM71285QC100-7 PM71285QC100-10 PM71285QC100-15	5.0V 5.0V 5.0V 5.0V	128 128 128				
PM71285L284-10 PM71285QC100-6 PM71285QC100-7 PM71285QC100-7 PM71285QC100-10 PM71285QC100-15 Companion device	5.0V 5.0V 5.0V	128 128 128			v T	
PM 71285L84-10 PM 71285QC100-6 PM 71285QC100-7 PM 71285QC100-7 PM 71285QC100-10 PM 71285QC100-15 Companion device HardCopy:	5.0V 5.0V 5.0V 5.0V	128 128 128			~	





5、设置综合、仿真、时序分析软件,在此可以捆绑第三方工具, 本次实验,选用软件自带的工具,按Next继续。

	Synthesis			
Tool name:	<none></none>			•
Format:				v
□ Run this	tool automatically to syr	nthesize the current desi	gn	
Simulation				
Tool name:	<none></none>			•
Format				-
🗖 Run gate	level simulation autom	atically after compilation		
	is			
Timing Analus	10			•
Timing Analys Tool name:	<none></none>			
Timing Analys Tool name: Format:	<none></none>			 -
Timing Analys Tool name: Format:	<none></none>	compilation		<u>*</u>
Timing Analys Tool name: Format:	<pre></pre>	compilation		<u></u>
Timing Analys Tool name: Format:	None> tool automatically after	compilation		<u>*</u>





6、设置参数的总结,按Finish完成project的建立。

When you click Finish, the project w	ill be created with the following settings:	
Project directory:		
C:/Users/Dongwei/Desktop/P	LD/test1/	
Project name:	test1	
Top-level design entity:	test1	
Number of files added:	0	
Number of user libraries added:	0	
Device assignments:		
Family name:	MAX7000S	
Device:	EPM7128SLC84-7	
EDA tools:		
Design entry/synthesis:	<none></none>	
Simulation:	<none></none>	
Timing analysis:	<none></none>	
Operating conditions:		
Core voltage:	5.0V	
Junction temperature range:	0-85 癈	





1、File ->new,选择新建一个BDF文件

Quartus II - C:/Users/Dongwei/Desktop/PLD/test1/test1 - test1 - X	New
rrie toit view project assignments processing tools window nep □ New Ctrl+N © Open Ctrl+P4 ⊆lose Ctrl+F4	
New Project Wizard Open Project Ctrl+J Convert MAX+PLUS II Project Save Project Save Ctrl+S Save Ctrl+S Save Current Report Section As File Properties Crate / Update Export Convert Programming Files Page Setup Print Pregiew Print Ctrl+P	AHDL File Block Diagram/Schematic File EDIF File State Machine File SystemVerilog HDL File Tol Script File Verilog HDL File VHDL File VHDL File Wenory Files Memory Initialization File Memory Initialization File System Sources and Probes File Logic Analyzer Interface File SignalTap II Logic Analyzer File Vector Waveform File
Recent Projects Image: Control of the second seco	HDL Include File
	Chain Description File Synopsys Design Constraints File Text File
System & Processing & Extra Info & Info & Warning & Critical Warning & Error & Suppressed & Flag /	OK Cancel





2、建立and3 符号







3、相同操作添加 input 和 output 管脚,并连线







4、修改管脚名(可选),而后编译







5、可查看各种报告,尤其是时序分析

	Compilation Report - Flo	w Summ
Compilation Report Legal Notice Flow Summary Flow Settings Flow Non-Default Global Flow Elapsed Time Flow Log Analysis & Synthesis Fitter Assembler Timing Analyzer	Flow Summary Flow Status Quartus II Version Revision Name Top-level Entity Name Family Device Timing Models Met timing requirements Total macrocells Total pins	Successful - Wed Sep 21 19:12:48 2022 8.0 Build 215 05/29/2008 SJ Full Version test1 test1 MAX7000S EFM7128SLC84-7 Final Yes 1 / 128 (< 1 %) 8 / 68 (12 %)





6、分配管脚,分配管脚前需要编译一次,Assignments -> Pin Planner 或者 Assignments -> Assignment Editor -> Category 中选择 Pin







7、保存分配管脚的文件, 日后重建 project 时可直接导入不需点击分配 [♥] Quartus II - C:/Users/Dongwei/Desktop/PLD/test1-test1 - [Pin Planner]

æ	Export					
\$	保存在(I):	test1		• + (• ⊡ * ⊡	
· 昭 離 · · · · · · ·	快速访问 桌面 桌面 上地电脑	名称 db	^		修改日期 2022/9/21 19:12	
₽	网络		保存文件			
_		文件名(N):	test1.csv		- Expo	rt
		保存类型(T):	Comma Separated Value	e File (*.csv)	· ▼ 取消	¥





8、分配完再编译一次

? 5	E 🕨 Com	pile Design
?	÷ ►	Analysis & Synthesis
?	÷ ►	Fitter (Place & Route)
?	÷ ►	Assembler (Generate programming files)
?	÷ ►	Classic Timing Analysis

🗸 E	🕨 Compile Design	
~	🗄 🕨 🕨 Analysis & Synthesis	
~	🗄 🕨 Fitter (Place & Route)	_
~	🗄 🕨 🕨 Assembler (Generate programmin	g files)
~	🗄 🕨 Classic Timing Analysis	





步骤三 时序仿真与功能仿真

1、File->new, Vector Waveform File, 点击 ok







2、新建用于仿真的波形文件



Insert Node	or Bus	×	Node Finder		1、列出所	府节点	
<u>N</u> ame:		ок	Named: * Look in: [test] Nodes Found: Name	Filter: Pins: assigned	Customize Customize	List	OK Cancel
<u>T</u> ype:	INPUT 💌	Cancel	in1 in2 in3 in3 in3	PIN_4 I PIN_5 I PIN_5 I PIN_66 I PIN_8 (PIN_8	ljin1 ljin2 ljin3 ljout	PIN_4 I PIN_5 I PIN_6 I PIN_9 (
⊻alue type:	9-Level	Node <u>Finder</u>			Toat	rin_o (
<u>R</u> adix:	ASCII	添加节点		») 2,	选择所有节点		
Bus <u>w</u> idth:	1	NUMBER 12 MIX					
Start jndex:	0						
🔲 Display gi	ray code count as binary count		<	> <		>	



步骤三 时序仿真与功能仿真

3、设置仿真时间, Edit -> End Time, 设置合适的时间

ault extension of ension value: [[ptions: _ast clock pati	tern	•
time extension	per signal:		
Signal Name	Direction	l Radix	Extension value
in1	Input	ASCII	Default extension value
in2	Input	ASCII	Default extension value
in3	Input	ASCII	Default extension value
out	Output	ASCIL	Default extension value



步骤三 时序仿真与功能仿真

4、设置 Grid Size(Edit -> Grid Size),而后设置输入信号波形







5、进行时序仿真, Processing -> Simulator Tool

➡ Simul¶tor 选	择mode为Timing	-	
Simulation mode:	Timing 🗾 👻	Generate Fund	ctional Simulation Netlis
Simulation input:	test1.vwf		Add Multiple Files
- Simula <mark>ßo</mark> n pe jige Run simulatio C End simulatio	<mark>我 .vwf 文件, 会自动</mark> n until all vector stimuli are used n at: 100 ns	加载	
- Simulation options Automatically Check output Setup and ho Glitch detecti	Quartus II a s lc or	× uccessful	<
C Overwrite sim	u r	确定	
Generate VCI) File:		
3、star	0 % 00:00:00		
≿ Start	1 Stop	🕑 Open 📗	Report





6、点击 Report 查看时序仿真结果







7、保存仿真文件 File -> Save Current Report Section As





步骤三 时序仿真与功能仿真

8、进行功能仿真, Processing -> Simulator Tool

Similato选择 mode 为 Functional 3、生成网表 🖾	
Simulation mode Functional 💽 Generate Functional Simulation Netlist	
Simulation input: test1.vwf Add Multiple Files	
Simulatio们就需要注意加载的是否是你期望的 vwf 文件 • Run simulation until all vector stimuli are used	Quartus II X
C End simulation at: 100 ns 💌	Functional Simulation Netlist Generation was successful
Simulation options	
Automatically add pins to simulation output waveforms	[r
Check outputs Waveform Comparison Settings	确定
Setup and hold time violation detection	
🖵 Glitch detection: 1.0 ns 💌	Quartus II X
Cverwrite simulation input file with simulation results	
🗖 Generate Signal Activity File:	
Generate VCD File:	Simulator was successful
4、Start 00.00.01 5、查看功能仿真结果	确定
🚬 Start 🛛 🐨 Stop 🕸 Open 🔮 Report	





9、点击 Report 查看时序仿真结果





步骤三 时序仿真与功能仿真

10、保存仿真文件 File -> Save Current Report Section As







1、单独的原理图文件(*bdf)是无法编译的。需要把原理图文件添加 到工程中(如果遵循先新建工程,再建立原理图文件,则原理图文件会 自动添加到工程中。否则,需要手动添加)。

2、新建原理图文件时,保存的文件名要与工程名相一致。注意不要与 Quartus II自带的符号(Symbol)库里的函数名(如and3、dff及74138等) 重复。

3、如果建立的仿真文件(*vwf)多于一个,需要手动指定仿真哪个文件(方法: Assignments - Settings - Simulator Settings - Select simulation options - Simulation input)。否则,系统默认仿真最先建立的那个仿真文件。





Project -> Archive Project,将工程存档,生成.qar的文件后,与实验报告 一并提交。

实验课程网址: http://home.ustc.edu.cn/~dwzou/

